MSC7104 GPON:
Integrated GPON ONT System-on-Chip

Overview

The MSC7104 GPON is a System-on-Chip (SoC) solution for broadband passive optical network termination (ONT) applications. It integrates a GPON TC/MAC, Gigabit Ethernet (GbE) TC/MACs and a clock and data recovery (CDR) unit to a core built on Power Architecture® technology.
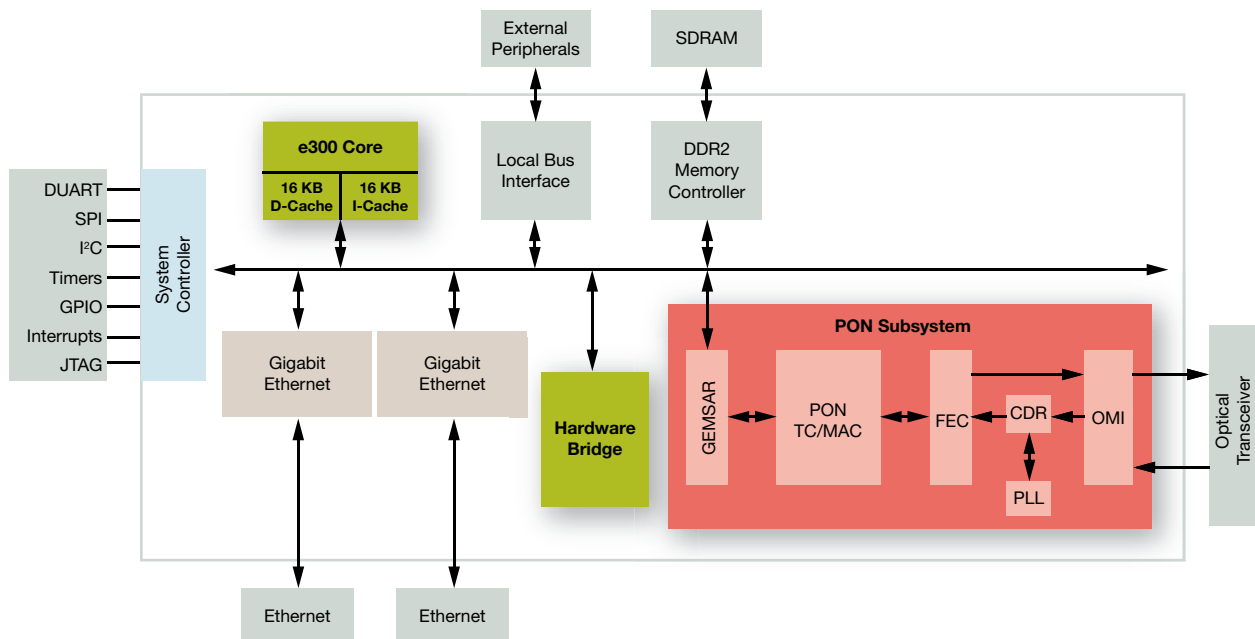
The MSC7104 GPON provides a highly integrated solution designed to minimize ONT costs through silicon integration and a reduction of external components. The MSC7104 GPON SoC device is based on Freescale's e300 processor platform built on Power Architecture technology, which provides the foundation for the company's

PowerQUICC® II Pro communications processor family. The MSC7104 GPON device's e300 core operates at 266 MHz and includes a 16 KB instruction cache and a 16 KB data cache. The SoC integrates a DDR2 memory controller, a PowerQUICC II-compatible local bus controller, two 10/100/1000 Ethernet controllers, a dual universal asynchronous receiver/transmitter (DUART), I²C, a serial peripheral interface (SPI), an interrupt controller and parallel general-purpose input/outputs (GPIOs).

The PON subsystem is based on a GPON layer termination device as specified in ITU-T G.984. The PON subsystem integrates the TC/MAC function as well as the CDR

function; it further supports Advanced Encryption Standard (AES), Forward Error Correction (FEC) and dynamic bandwidth reporting per the FSAN requirements. A hardware bridge ensures that a high-throughput data path is available with minimum intervention required by the e300 core. Further, the PON subsystem leverages Freescale's leadership in B-PON products and mixed-signal technology. Built on third-generation Freescale PON technology, the MSC7104 is a cost-reduced version of the groundbreaking MSC7120 device that has been deployed in large volumes worldwide. It features proven interoperability with many of the world's top carriers.

MSC7104 GPON Block Diagram

freescale™
semiconductor

MSC7104 GPON Features

PON Subsystem

- Integrated CDR
- Support for GPON mode per ITU-T G.984.1, 984.2, 984.3 and 984.4 standards
- Down/upstream rate: up to 2.4 Gbps/1.2 Gbps
- Upstream traffic scheduler
- Support for up to 38 allocation IDs and 39 port IDs
- 64-entry IP group address filter for in-line video distribution support

Hardware Bridge

- Filters and forwards packets between the e300 and two GbE TC/MACs with no processor overhead
- Video packets switched in hardware with no processor overhead

e300 Power Architecture Core Processor

- 32-bit, high-performance, superscalar processor core
- 511 Dhrystone 2.1 MIPS at 280 MHz (1.92 DMIPS/MHz) with 16 KB I/D-caches
- Load/store, system register and branch processor units and two integer units
- Dynamic power management

DDR2 Memory Controller

- 32-bit data interface, up to 280 MHz data rate
- Page mode support for up to four simultaneous open pages

Dual 10/100/1000 Ethernet TC/MAC Controllers

- Two 10/100/10000 Ethernet interfaces with GMII, RGMII, MII and FIFO8 physical interfaces
- Each TC/MAC supports eight priority transmit/receive rings, transmit scheduler/receive filer
- L2, L3 and L4 filing, VLAN tag insertion and extraction

Local Bus Controller

- 26-bit address bus and 16-bit/8-bit data bus and data operating up to 66 MHz
- 8-bit and 16-bit port sizes controlled by on-chip memory controller

Peripherals, Miscellaneous I/Os

- DUART
- I²C and SPI interfaces
- TDM port available for DSP functions
- JTAG test access port
- Up to 48 parallel GPIOs

Technology

- 90 nm, 1.0V core and 1.8/2.5V I/O
- 456 TEPBGAII, 35 mm x 35 mm, 1.27 mm pitch

Software and Systems Enablement Support

e300 Power Architecture Software and Support

- Linux® operating system, standard TCP/IP stack ported
- Drivers for bridge, LAN and PON

Systems Enablement

- Reference design kit, debug environment
- ONT Management and Configuration Interface software reference stack from OpenCon Systems

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com/PON**.

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